## Amendments to the Specification

**Please replace the paragraph that begins on line 1, page 7, of the specification with the following amended paragraph:**

**FIG. 2A** shows a semiconductor device **150** isolated from external noise by a low resistive path barrier **152** and deep trench isolation **154** according to an embodiment of the present invention. The semiconductor device **150** may be a NMOS, a PMOS, a CMOS, a BiCMOS, and the like. The semiconductor device **150** may be formed on a conductivity region **156** (i.e., well region). The conductivity region **156** may actually include more than one type of conductivity region such as both an n-type and a p-type conductivity region. A low resistive path barrier **152** surrounds the conductivity region **156** isolating the conductivity region **156** from the underlying substrate **158**. Depending on the type of semiconductor device **150** (e.g., NMOS, PMOS, and the like), the substrate **158** may be biased to the highest or lowest (typically 0 volts) voltage possible. For the embodiment, the low resistive path barrier **152** may be coupled to a power supply **160**. The substrate **158**, among other things, supporting the semiconductor device **150** and the conductivity region **156** and may be either a p-type or an n-type substrate. The low resistive path barrier **152** may comprise of N+ or P+ material. The "+" designation is meant to indicate that the N or P doped material is highly doped. For example, according to some embodiments, the low resistive path barrier **152** may have doping concentration in the order of ten times the concentration of the conductivity region **156**. However, in other embodiments, the low resistive path barrier **152** may have even higher or lower doping concentrations. The low resistive path barrier **152** may be coupled to a power supply **160**, such as a DC power supply. A deep trench isolation **154** surrounds the low resistive path barrier **152** extending down into the substrate **158**. The deep trench isolation **154** may be filled with a dielectric or insulation material. Note that the low resistive path barrier **152** surrounds the conductivity region **156** in a manner such that in addition to isolating the conductivity region **156** and the semiconductor device **150** from the underlying substrate **158**, isolates the conductivity region **156** and the semiconductor device **150** from the deep trench isolation **154**.